REDUCING SILICON-SUBSTRATE PARASITICS OF ON-CHIP TRANSFORMERS

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ABSTRACT

Three-terminal transformers have been fabricated on 20-μm-deep silicon-oxide blocks formed in the silicon substrate. The thick isolation blocks drastically reduced the parasitics between the devices and the silicon substrate underneath. The quality factors and the self-resonant frequencies were thus increased by more than 100% and 70%, respectively. Such oxide blocks also greatly reduce the cross talk between adjacent devices by as much as 15dB.

INTRODUCTION

Monolithic transformers have found extensive applications in radio-frequency (RF) circuits in wireless communication systems, such as impedance matching, signal coupling, phase splitting and formation of large inductances on the order of tens of nanohenries [1-5]. Implemented in CMOS technology, the current transformers generally have low quality factors (Q), low self-resonant frequencies (f_{res}) [3-5] and large cross talk [6].

The low performance of current transformers is in part due to the parasitics between the devices and the lossy silicon substrate. First, the eddy currents induced in the silicon substrate beneath a transformer by the magnetic field generated in the device cause energy loss and reduce Q; this effect is especially serious at high frequencies, because the intensity of the eddy currents is proportional to the rate of change in the magnetic field. Second, the parasitic capacitances between the transformer traces and the substrate are in shunt with the inductance obtained from the spiral traces, thus lowering f_{res} of the transformer; these parasitic capacitances also enable electric coupling between the device and the substrate, causing further energy loss. Lastly, but not the least important, adjacent devices are coupled through these parasitics and their ambient (including both the substrate and air), hence large cross talk.

Because spiral inductors are typically used to form transformers, the very nature of coupling entails even greater parasitic capacitances and eddy currents among the spirals, resulting in more energy loss. Therefore, to improve the performance of the on-chip monolithic transformers, the parasitics due to the substrate should be suppressed as much as possible. One efficient approach is to drastically increase the thickness of the isolation layer, typically silicon dioxide (SiO_2), between the transformer and the silicon substrate. In doing so, the magnetic and electric coupling between the device and the silicon substrate and the coupling among devices through the substrate are greatly weakened.

In this paper we demonstrate the improvement in the performance of monolithic transformers with underlying deep SiO_2 blocks created by a MEMS process module. The depth of such oxide blocks is 20 μm. Simple two-layer three-terminal transformer structures formed by two metal layers were designed, fabricated and characterized as the testing devices.

FABRICATION

A. Formation of Deep SiO_2 Block

The deep silicon-oxide block was formed utilizing a MEMS process module developed in our group [7-9]. The whole procedures consisted of the following steps:

1. Etching 20-μm-deep periodic narrow beam-and-trench structures in the silicon substrate by deep reactive ion etching (DRIE);
2. Thermally oxidizing the silicon beams completely;
3. Depositing low temperature oxide (LTO) to seal the openings left after the oxidation;
4. Planarizing the surface of such an oxide block by chemical mechanical polishing (CMP) so that later process steps could proceed from a flat surface.

In the first step, the area where the SiO_2 block was to be placed was defined. Meanwhile, by etching those narrow beam-and-trench structures, the task of forming the SiO_2 block switched from growing thick SiO_2 in the direction normal to the substrate to that growing SiO_2 parallel to the substrate surface to form individual much thinner SiO_2 blocks. Therefore, through the second and third step, the block was formed with relatively thin SiO_2 layers. Fig. 1 shows the SEM image of the cross section of an oxide block. Because the LTO deposition was nonconformal, the trenches were only sealed, not completely *filled*; air voids were thus left within the block, shown in Fig. 1. These air voids should not harm the performance of the transformers; in fact, the combination of air and SiO_2 results in smaller parasitics than does SiO_2 alone, because the permittivity of air is less than that of SiO_2.

The 20-μm-deep SiO_2 blocks serve as the first isolation layer in the transformer structures. As we intended to study the effect of thick underlying silicon-oxide blocks on the transformer performance, the transformers were also fabricated without the underlying oxide blocks. The corresponding thickness of the isolation oxide, t_{ox}, was 4.1 μm, after wet oxidation, silicon-oxide deposition and CMP.

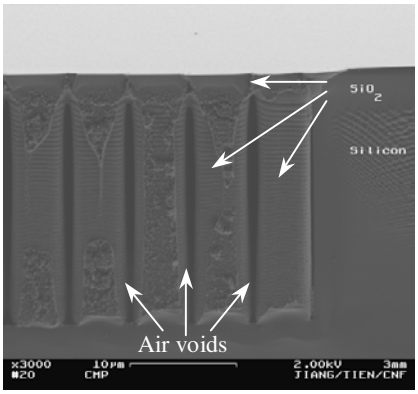

Fig.1 SEM image of the cross section of a 20-μm-thick SiO_2 block.

B. Fabrication of Transformer Structures

The transformers consisted of spirals and bridges that connected the center of the spiral across the spiral traces to the ground or probing pads. The structures were built on the first SiO_2 isolation layer and comprised two 1.4-μm-thick aluminum (Al) layers and a 1.4-μm-thick polyimide film in between as insulation. Table 1 lists the process parameters. The Al films were sputtered, patterned and wet etched to form the metal traces and bridges. The major benefit of using polyimide lies in its planarization capability; the variation in the topography can be sufficiently reduced after it is spun onto the wafer and cured and no other planarization step such as CMP is required. As shown in Table 1, the nominal thickness of the polyimide, t_{PI}, was 2.4 μm, while that between the two Al structures was in the range of 1.2 to 1.5 μm.

Table 1 Process parameters for the transformers.

t_{ox} (without block)	4.1 μm
t_{ox} (with block)	20 μm
t_{Al}	1.4 μm
t_{PI} (nominal)	2.4 μm
t_{PI} (between Al structures)	1.2 ~ 1.5 μm

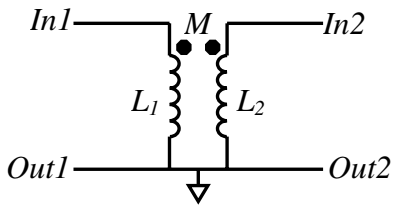

Fig. 2 Circuit model of a three-terminal transformer. The output ends of both windings are grounded.

TRANSFORMER DESIGN

A monolithic three-terminal transformer consists of two rectangular spirals, the primary and secondary windings, respectively. Fig. 2 shows its circuit model. The coupling coefficient, k, is defined by $k = M / \sqrt{L_p L_s}$, where L_p and L_s are the self-inductances of the primary and secondary spirals, respectively, and M is the mutual inductance, which can be either positive or negative. For perfect coupling, k equals unity; in reality, however, k is generally smaller than 0.9 for monolithic transformers [5].

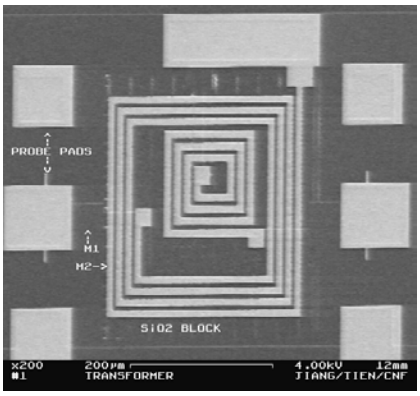

Fig. 3 SEM image of a three-terminal transformer in the encompassed configuration.

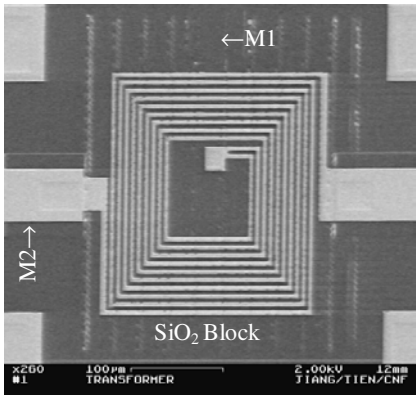

Fig. 4 SEM image of a three-terminal transformer in the intertwined configuration.

Table 2 Parameters of the transformers.

Parameters	*Int*	*Enc*
w (nominal | real in μm)	8 | 5	12 | 9
s (nominal | real in μm)	12 | 15	2 | 5
$n_p \mid n_s$	5 | 5	3.5 | 3.5
$d_p \mid d_s$ (μm)	85 | 100	45 | 200
w_b (nominal | real in μm)	20 | 17	
L_p (nH)	1.5	5.4
L_s (nH)	5.5	6.3
k	0.20	0.82

Two configurations of the primary and secondary spirals, encompassed and intertwined, were designed to form three-terminal transformers to study the effect of the deep SiO_2 blocks. In an encompassed configuration, one large spiral completely encloses a small one (Fig. 3); arbitrary turn ratio between the two spirals can be reached in this manner. An intertwined configuration means that two spirals are formed using the same Al layer and are placed intertwined with each other (Fig. 4); this configuration provides high k. The physical parameters that are used to describe a transformer include:

n_p and n_s - numbers of turns of the primary and secondary spirals, respectively;
w - the width of the spiral traces;
s - the spacing between adjacent spiral traces;
d_p and d_s - the lengths of the innermost traces of the primary and secondary spirals, respectively;
w_b - the width of the bridges.
The values of the parameters of the two transformers designed and fabricated, labeled *Int*, and *Enc*, are listed in Table 2. The nominal line width was reduced by about 3 μm because of undercuts after Al wet etch.

EXPERIMENTAL RESULTS

A. Definition of Q

Because a transformer consists of two spirals, two *Q*s need to be defined because of the general asymmetry between the primary and the secondary windings. Based on the assumption that the output signal utilized is voltage in most applications, open-circuit input impedances are used to define *Q*s, given in

$$Q_{1(2)} = \frac{\mathrm{Im}(Z_{11(22)})}{\mathrm{Re}(Z_{11(22)})}.$$

B. Improvements in Q and f_{res}

On-wafer testing and deembedment were performed on the fabricated transformers with a network analyzer and microwave probes. The *Z*-parameters were then converted from the measured *S*-parameters. The physical values of the two transformers are listed at the end of Table 2. The self-inductances of the primary and secondary spirals, L_p and L_s, respectively, were calculated from the measured reactances. The magnetic coupling coefficient, k, was simulated using MEMCAD.

Table 3 Improvements in Q and f_{res} with oxide blocks.

Device	*Enc*		*Int*	
SiO_2 block	yes	no	yes	no
Q_{max} @ GHz (Z_{11})	10.1 @ 4.50	4.5 @ 2.0	4.8 @ 4.6	2.3 @ 2.5
Q_{max} @ GHz (Z_{22})	20.3 @ 12.4	5.7 @ 7.0	4.7 @ 4.4	2.2 @ 2.5
f_{res} (GHz)	9.8	5.7	10.0	5.6

The f_{res} of the transformer is the frequency at which Z_{11} or Z_{22} of the device first becomes purely resistive. Beyond this point, the device has a capacitive impedance looking into one end and no longer functions as a transformer. Fig. 5 plots Q against the frequency for *Enc*, with and without the silicon-oxide block, as an example. Table 3 summarizes the f_{res} and maximum Q for both *Enc* and *Int*. Both f_{res} and Q are increased significantly with the underlying 20-μm-deep SiO_2 block, because the parasitics are drastically reduced.

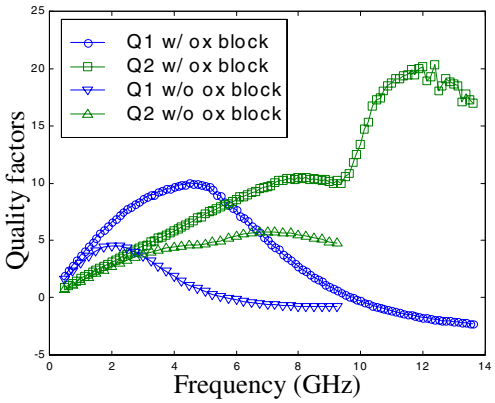

Fig. 5 Q of *Enc* with and without the 20-μm-deep oxide block. $Q_{1(2)}$ is calculated from $Z_{11(22)}$.

C. Reduction in Cross Talk

To study the effect of the underlying SiO_2 block on the cross talk among devices, two identical single-end inductors were placed 25 μm apart, as shown in Fig. 6. The cross talk between these two inductors can be characterized by S_{21}, the transmission coefficient between the two ends. Fig. 7 draws the magnitude of S_{21} against frequency in decibels (dB), with and without the oxide blocks; a reduction as large as 15 dB in $|S_{21}|$ was reached with such blocks.

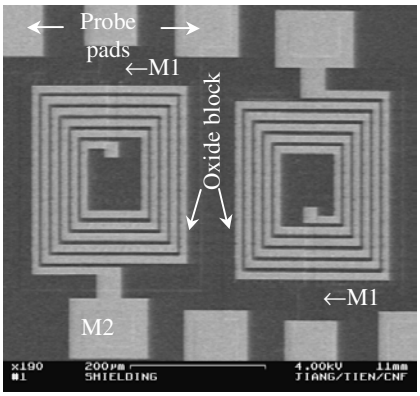

Fig. 6 SEM image of two adjacent identical spiral inductors built on 20-μm-thick SiO_2 blocks.

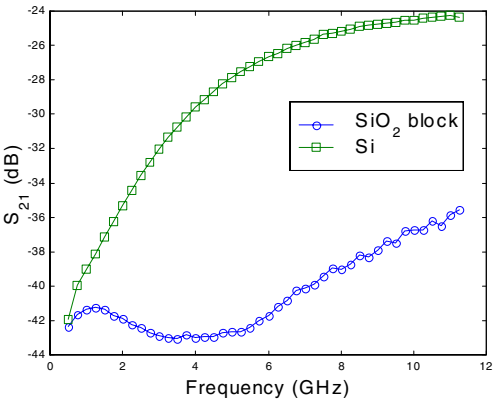

Fig. 7 Cross talk between two adjacent identical inductors with and without underlying SiO_2 block.

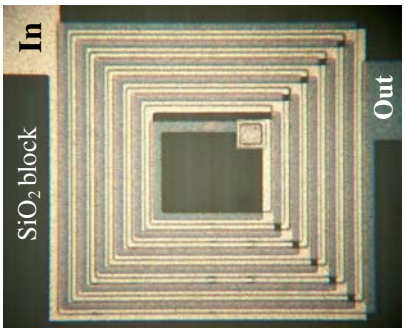

Fig. 8 Chip photograph of an inductor formed with two stacked identical spirals connected in series.

LARGE-INDUCTANCE INDUCTOR

An application of monolithic transformers described above is to form inductors with larger inductance. In our previous work described in [8], a single-level 8.2-nH spiral (excluding the bridges) occupies a chip area of 325 × 305 μm^2. For inductors of more than 10 nH, the area penalty with a single-level spiral would be forbidding. The mutual inductance between the two spirals of a transformer, on the other hand, can be employed to produce large inductance [3]. The two spirals of a three-terminal transformer can be connected in series; if the windings are such that the magnetic field generated in the two spirals is in the same direction, the inductance seen between the two input ends, L, is then given by

$$L = L_p + L_s + 2M = L_p + L_s + 2k\sqrt{L_p L_s} \qquad (1)$$

If $k \approx 1$ and $L_p \approx L_s$, then $L \approx 4 \times L_{p(s)}$. Therefore, inductance much larger than 10 nH can be achieved without much chip-area consumption. Fig. 8 shows the chip photograph of such an inductor, labeled *lind*. The primary and the secondary spirals are identical and are stacked, one on top of the other, for maximum M. Table 4 lists the physical parameters of the two identical windings.

Table 4 Parameters of the two spirals forming *lind*.

w (nominal | real in μm)	12 | 9
s (nominal | real in μm)	3 | 6
$n_{p(s)}$	6
$d_{p(s)}$ (μm)	80
w_b (nominal | real in μm)	20 | 17
L (nH)	6.7

Simulation of *lind* with MEMCAD gives $L_p = L_s = 6.7$ nH and $k = 0.84$. Hence the simulated inductance of *lind* is 24.7 nH, calculated from (1). The measured value from the reactance was 24.1 nH, consistent with the simulation. The die area consumed by this inductor was only 300×300 μm^2, including the underlying silicon-oxide block. Again, the silicon-oxide block significantly improves the performance of the inductor and the results are summarized in Table 5.

Table 5 Q and f_{res} of *lind* with and without the underlying oxide block.

	SiO_2 block	no SiO_2 block
Q_{max}	4.30 @ 1.63 GHz	1.78 @ 1.38 GHz
f_{res} (GHz)	3.20	2.44

CONCLUSIONS

We have applied a MEMS process module that creates 20-μm-deep silicon-oxide isolation blocks in the silicon substrate to drastically reduce the parasitics between the on-chip transformers and the underneath silicon substrate. The performance of the devices is thus greatly improved: Q is increased by more than 100% and f_{res} by more than 70%; cross talk between adjacent devices is reduced by as much as 15dB. This approach to reducing the silicon-substrate parasitics can potentially be integrated into IC processes for applications in RF circuits and wireless communication systems.

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REFERENCES

[1] P.R. Gray and R.G. Meyer, "Future directions in silicon ICs for RF personal communications," *Proc. IEEE CICC*, 1995, pp. 83-90.

[2] L.E. Larson, "Integrated circuit technology options for RFIC's – present status and future directions," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 387-399, March 1998.

[3] J. Zhou and D. Allstot, "Monolithic transformers and their application in a differential CMOS RF low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2020-2027, December 1998.

[4] A. Zolfaghari, A. Chan and B. Razavi, "Stacked inductors and transformers in CMOS technology," *IEEEJ. Solid-State Circuits*, vol. 36, no. 4, pp. 620-628, April 2000.

[5] J. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368-1382, September 2000.

[6] N.P. Pham, "A micromachining post-process module for RF silicon technology," *Proc. IEEE IEDM*, 2000, pp. 481-484.

[7] J.-L. Yeh, H. Jiang and N.C. Tien, "Integrated polysilicon and DRIE bulk silicon micromachining for an electrostatic torsional actuator," *J. Microelectromech. Syst.*, vol. 8, no. 4, pp. 456-466, December 1999.

[8] H. Jiang, Y. Wang, J.-L. A. Yeh and N.C. Tien, "On-chip spiral inductors suspended over deep copper-lined cavities," *IEEE Trans. Microwave Theory Tech.*, vol. 48, no. 12, pp. 2415-2423, December 2000.

[9] H. Jiang, *et al.,* "Fabrication of thick silicon-dioxide sacrificial and isolation blocks in silicon substrate," *J. Micromech. Microeng.,* in press.